



3/62

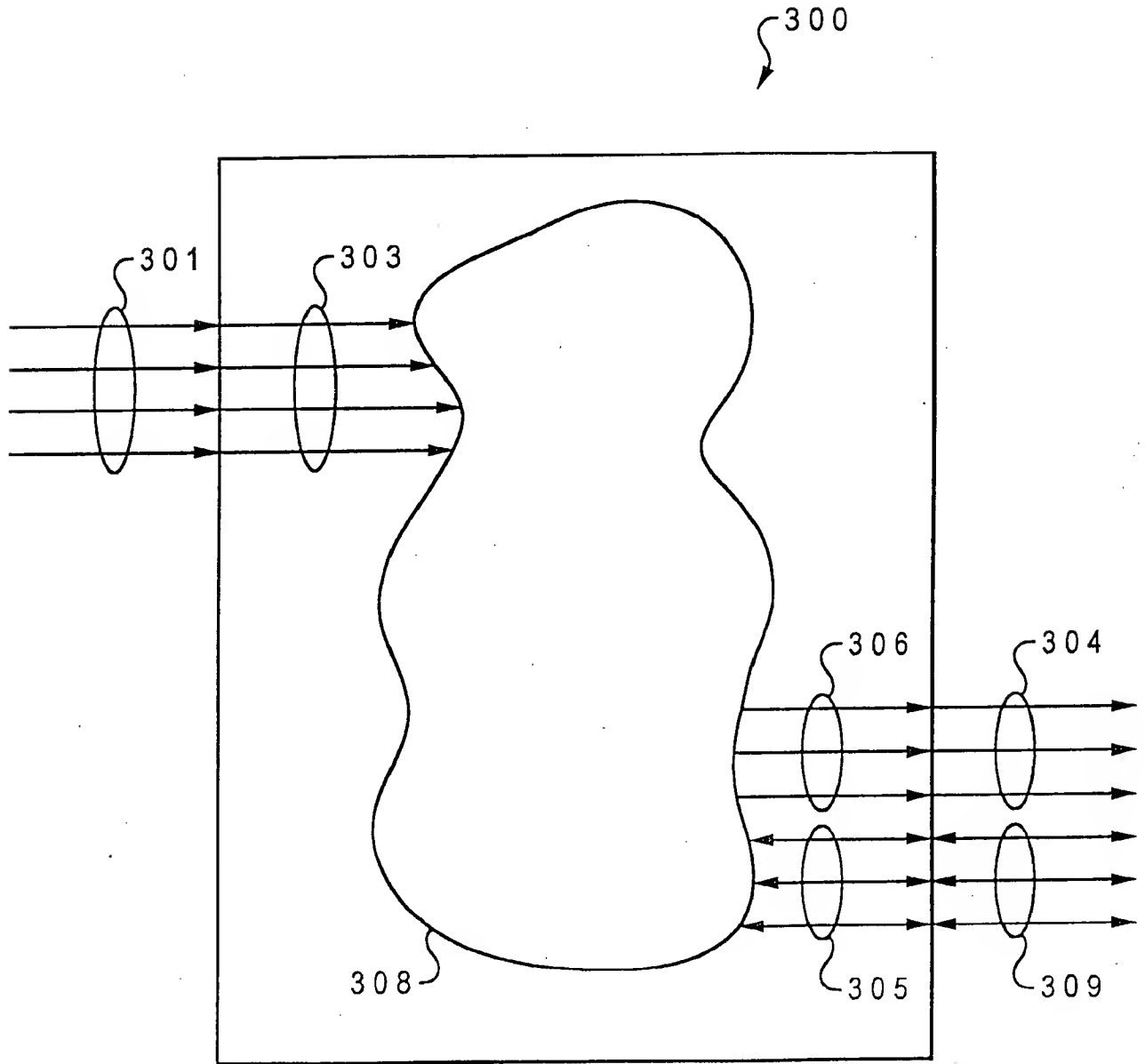


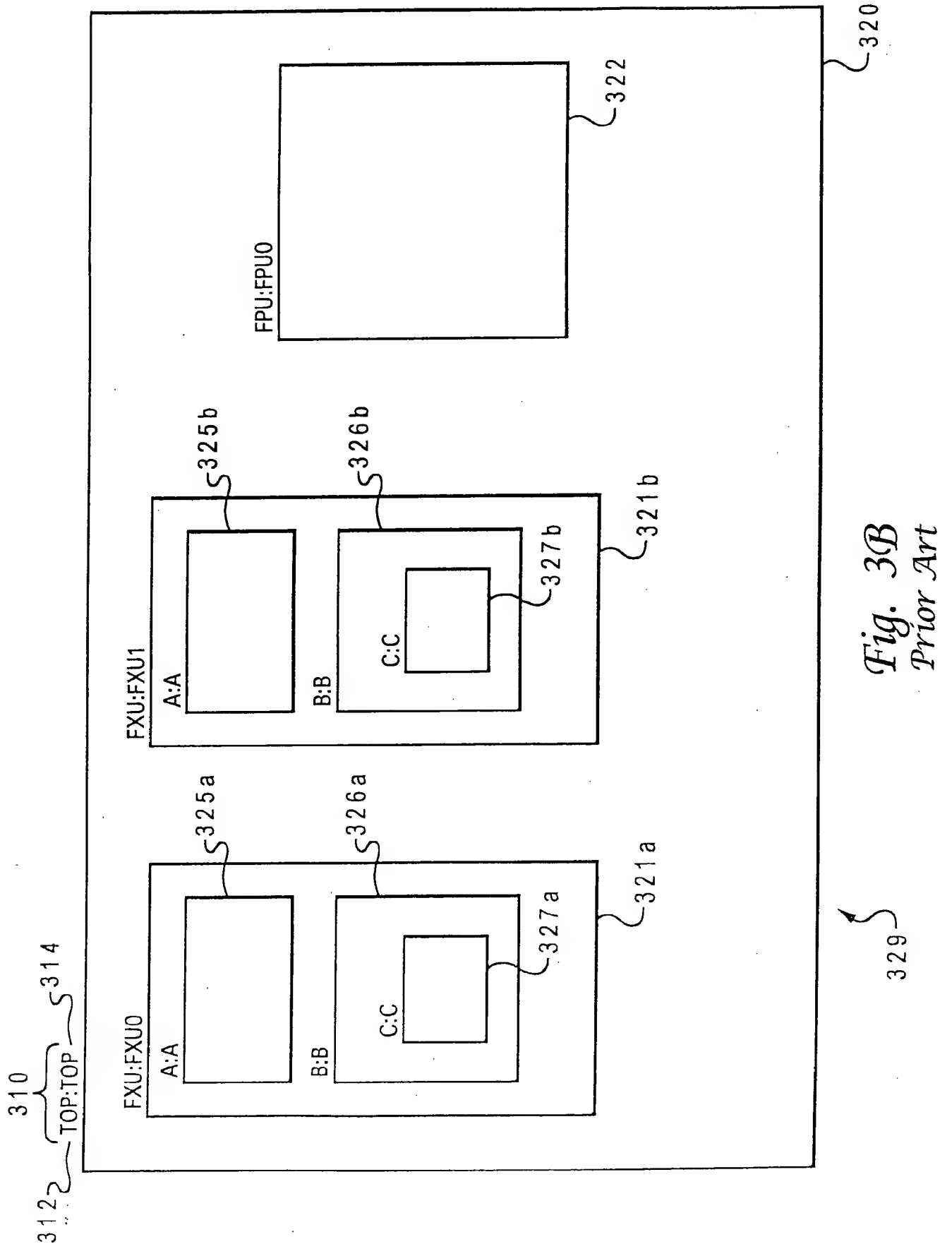
Fig. 3A
Prior Art

AUS920000651US1

Gabele, et al.

Non-Redundant Collection Of Harvest Events
Within A Batch Simulation Farm Network

4/62



5/62

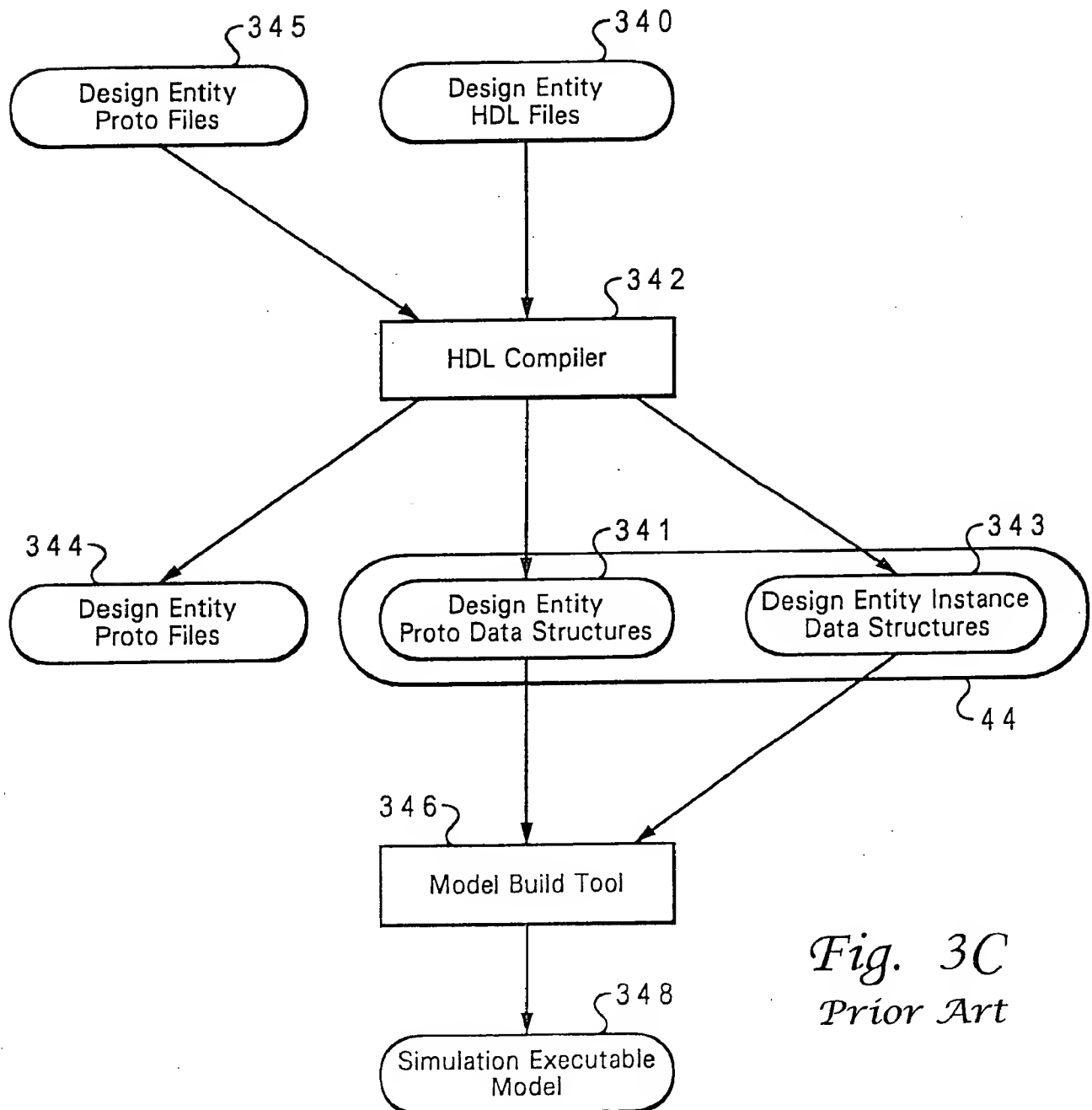


Fig. 3C
Prior Art

6/62

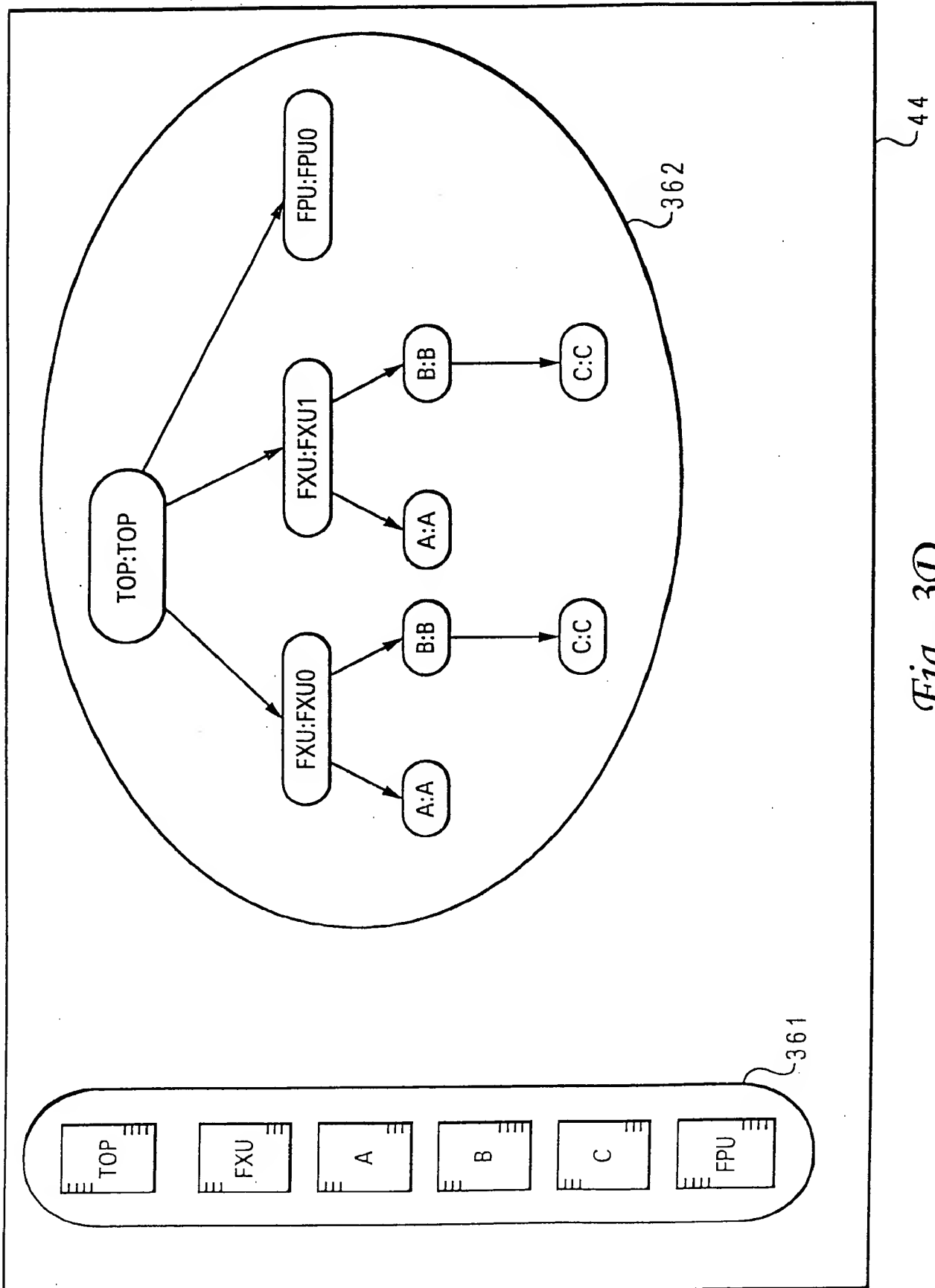


Fig. 3D
Prior Art

7/62

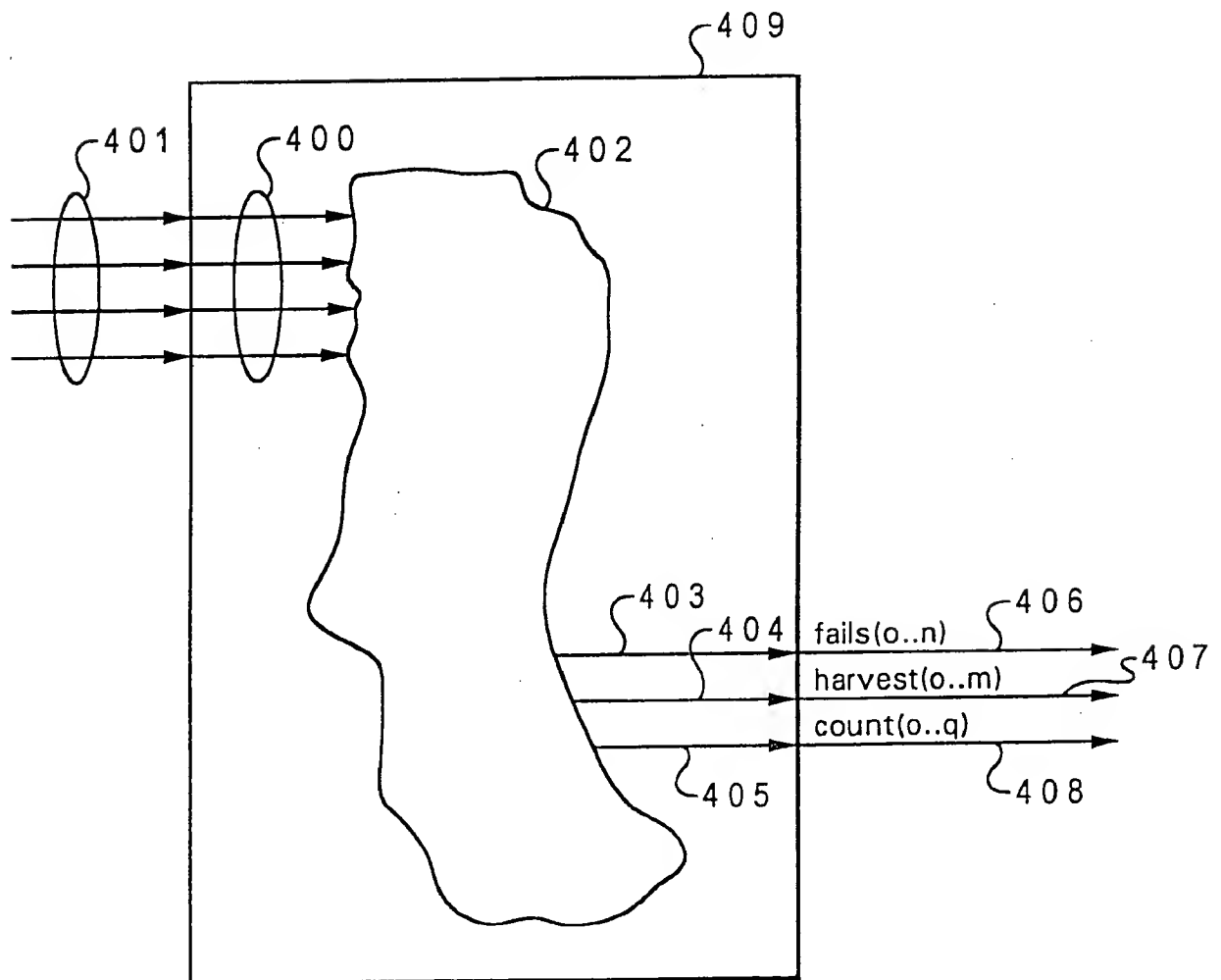


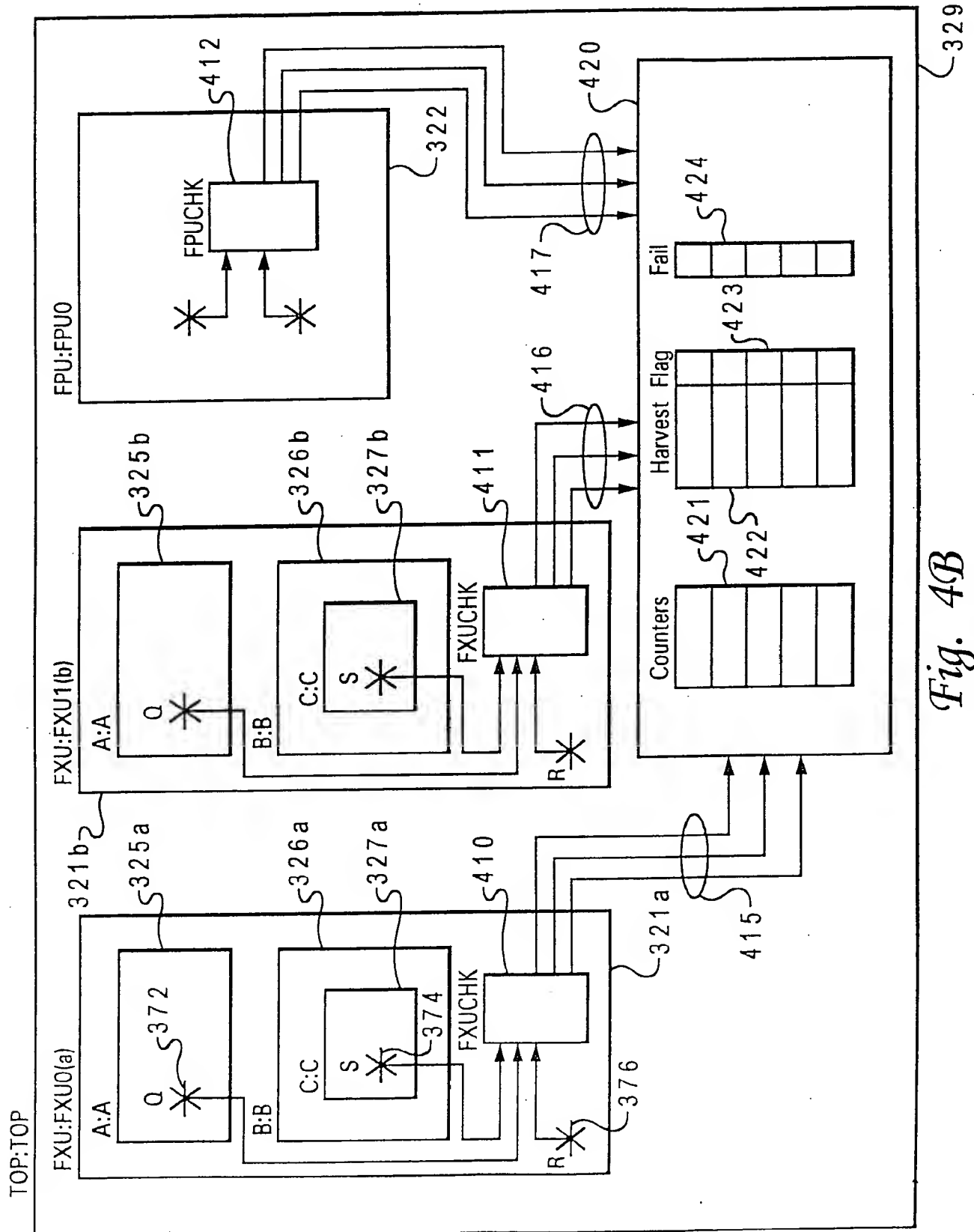
Fig. 4A
Prior Art

AUS920000651US1

Gabele, et al.

Non-Redundant Collection Of Harvest Events
Within A Batch Simulation Farm Network

8/62

Fig. 4B
Prior Art



9/62

```
ENTITY FXUCHK IS
    PORT(
        S_IN      : IN std_ulogic;
        Q_IN      : IN std_ulogic;
        R_IN      : IN std_ulogic;
        clock      : IN std_ulogic;
        fails      : OUT std_ulogic_vector(0 to 1);
        counts     : OUT std_ulogic_vector(0 to 2);
        harvests   : OUT std_ulogic_vector(0 to 1);
    );
4 5 2 { --!! BEGIN
      --!! Design Entity: FXU;
4 5 3 { --!! Inputs
      --!! S_IN      => B.C.S;
      --!! Q_IN      => A.Q;
      --!! R_IN      => R;
      --!! CLOCK     => clock;
      --!! End Inputs
4 5 4 { --!! Fail Outputs;
      --!! 0 : "Fail message for failure event 0";
      --!! 1 : "Fail message for failure event 1";
      --!! End Fail Outputs;
4 5 5 { --!! Count Outputs;
      --!! 0 : <event0> clock;
      --!! 1 : <event1> clock;
      --!! 2 : <event2> clock;
      --!! End Count Outputs;
4 5 6 { --!! Harvest Outputs;
      --!! 0 : "Message for harvest event 0";
      --!! 1 : "Message for harvest event 1";
      --!! End Harvest Outputs;
4 5 7 { --!! End;

ARCHITECTURE example of FXUCHK IS
    BEGIN
        ... HDL code for entity body section ...
    END;
```

4 5 0

4 5 1

4 4 0

4 5 8

Fig. 4C
Prior Art

10/62

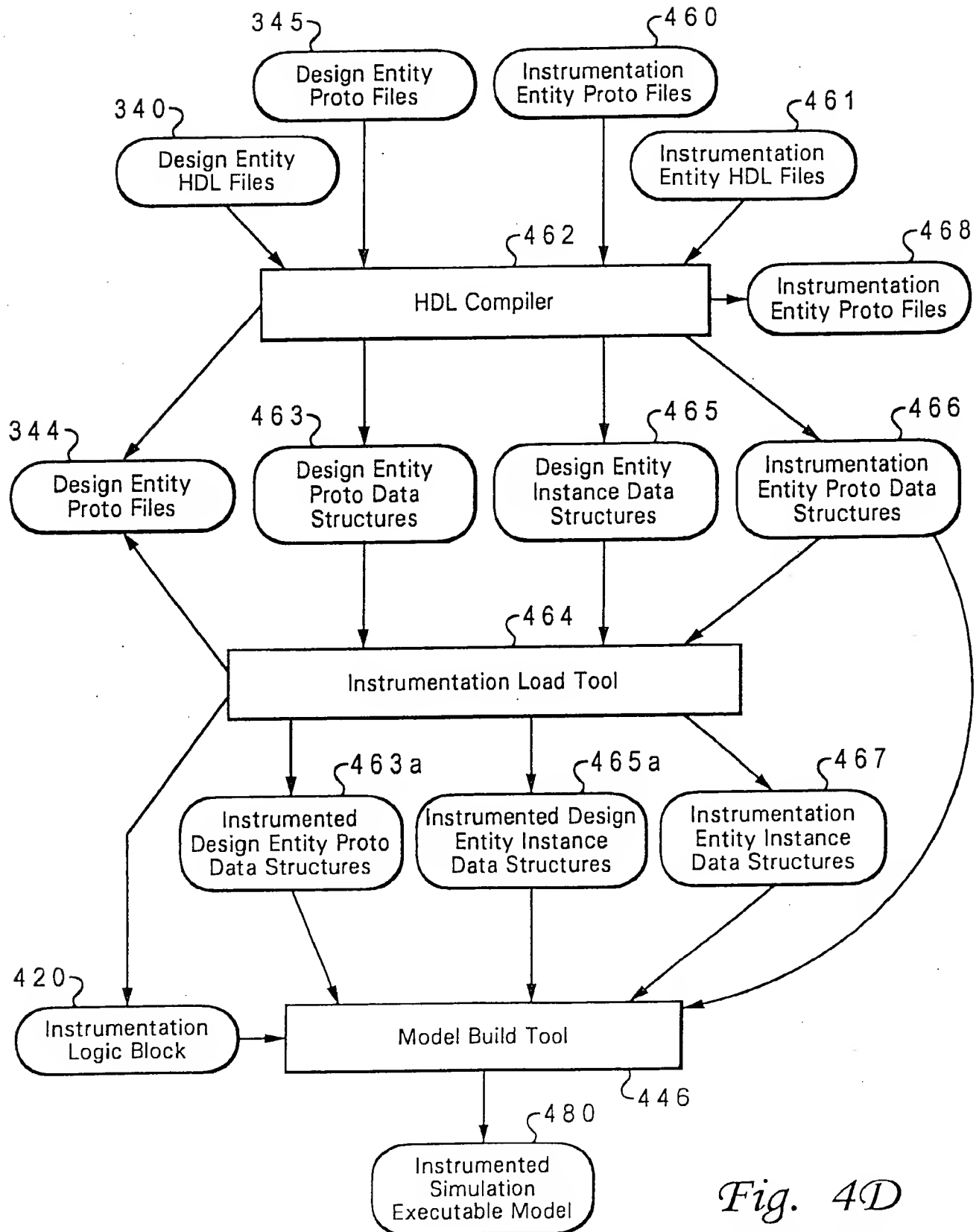


Fig. 4D
Prior Art

11/62

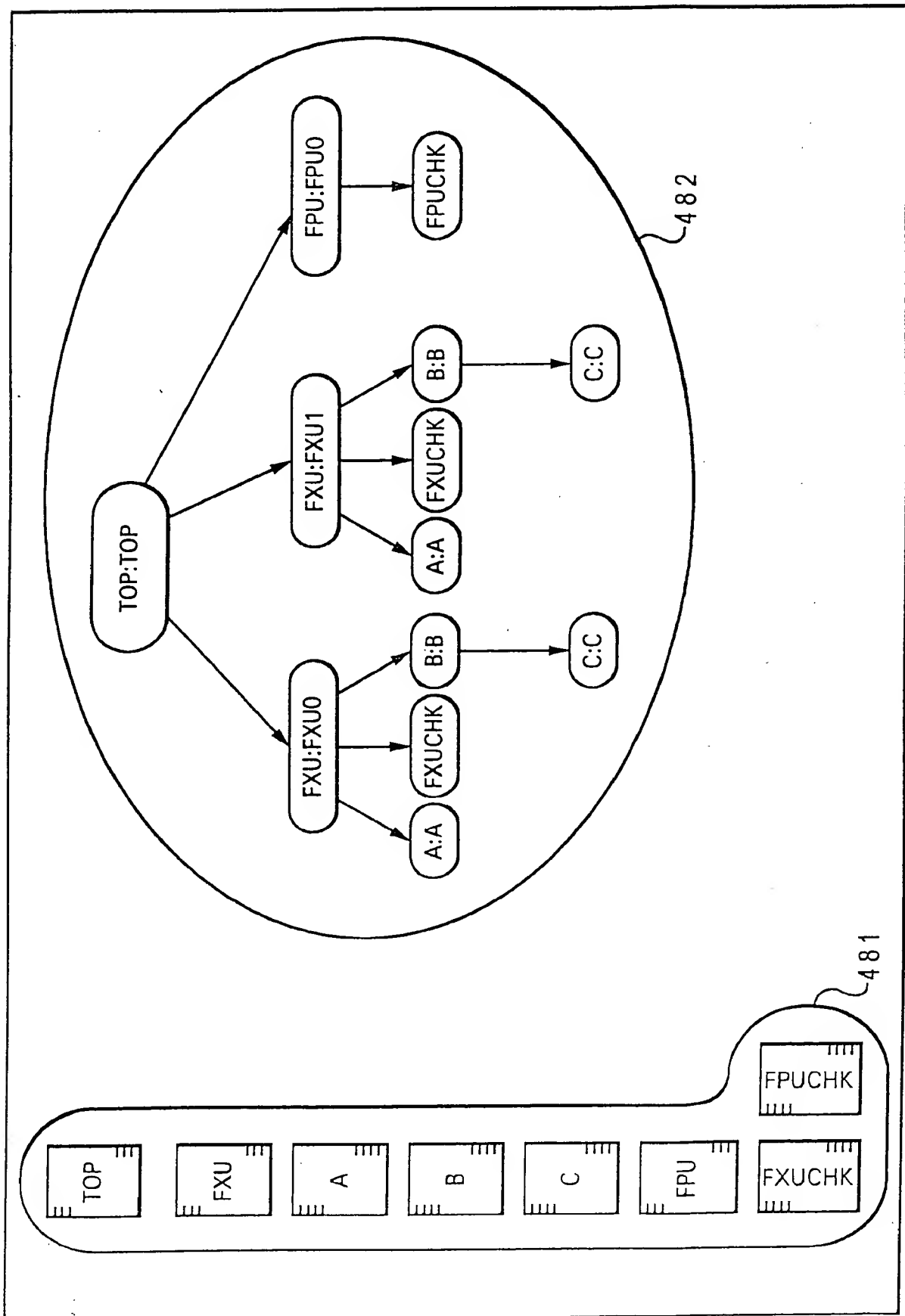


Fig. 4E
 Prior Art

AUS920000651US1
 Gabele, et al.
 Non-Redundant Collection Of Harvest Events
 Within A Batch Simulation Farm Network

12/62

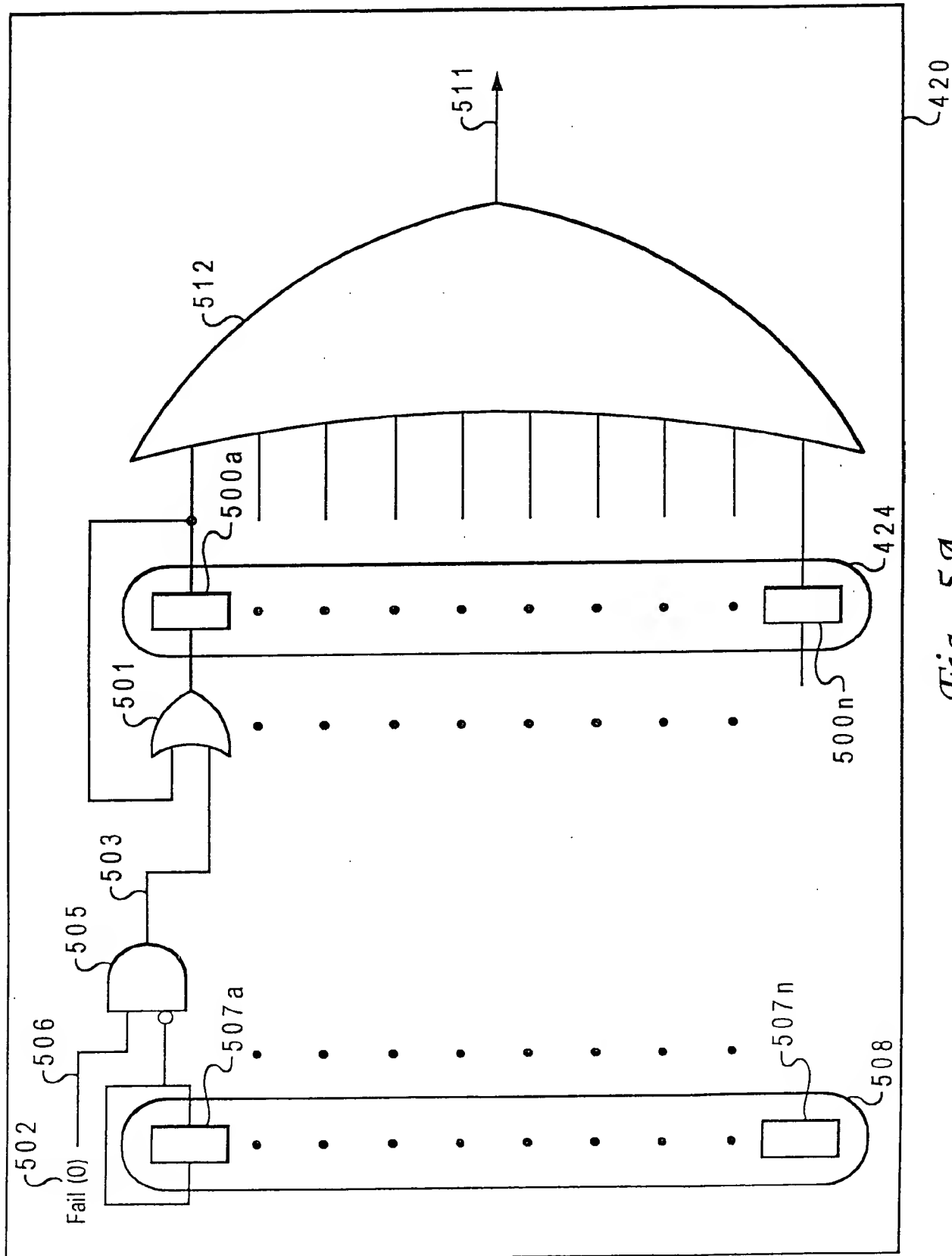


Fig. 5A
 Prior Art

13/62

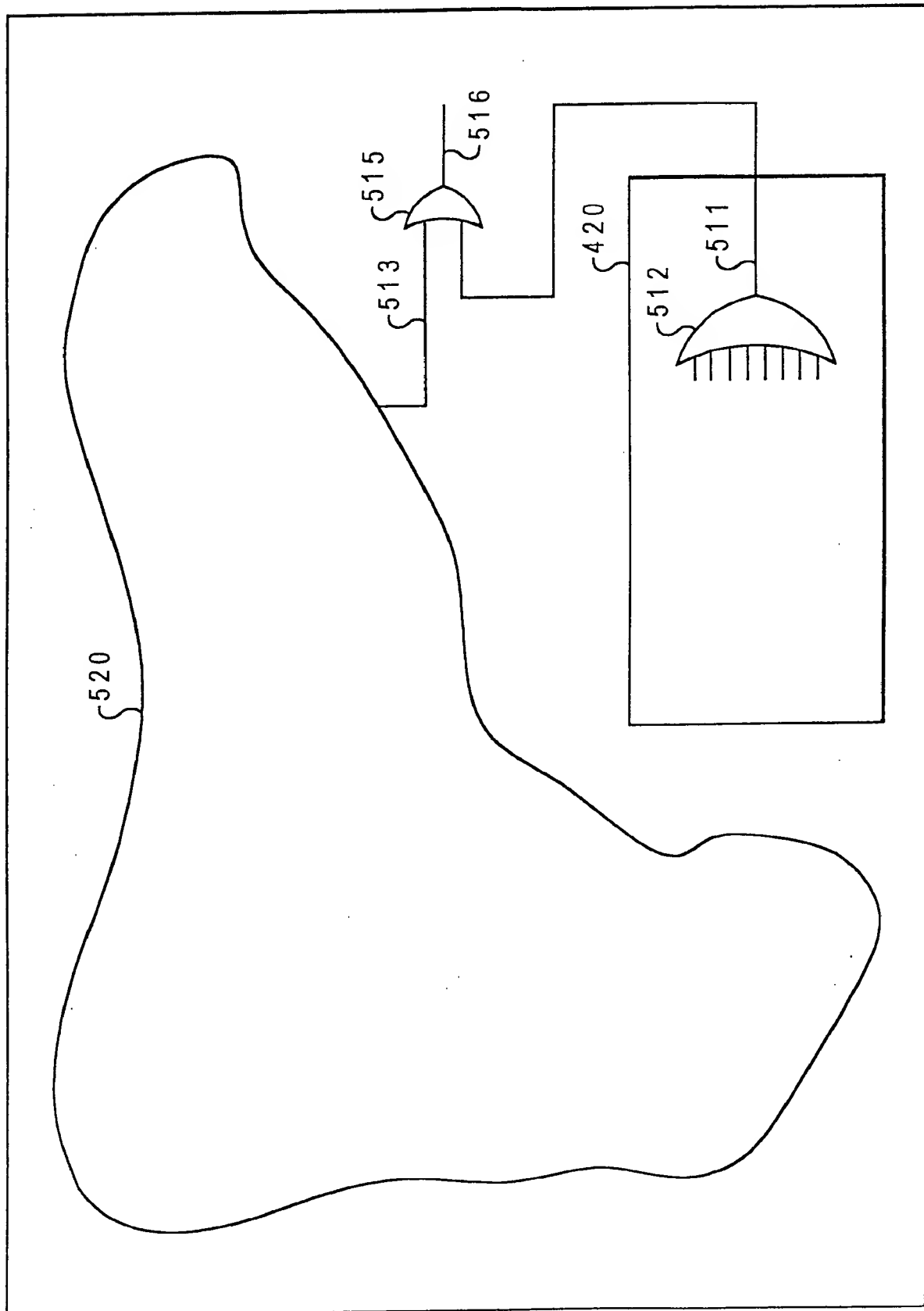


Fig. 5B
Prior Art

14/62

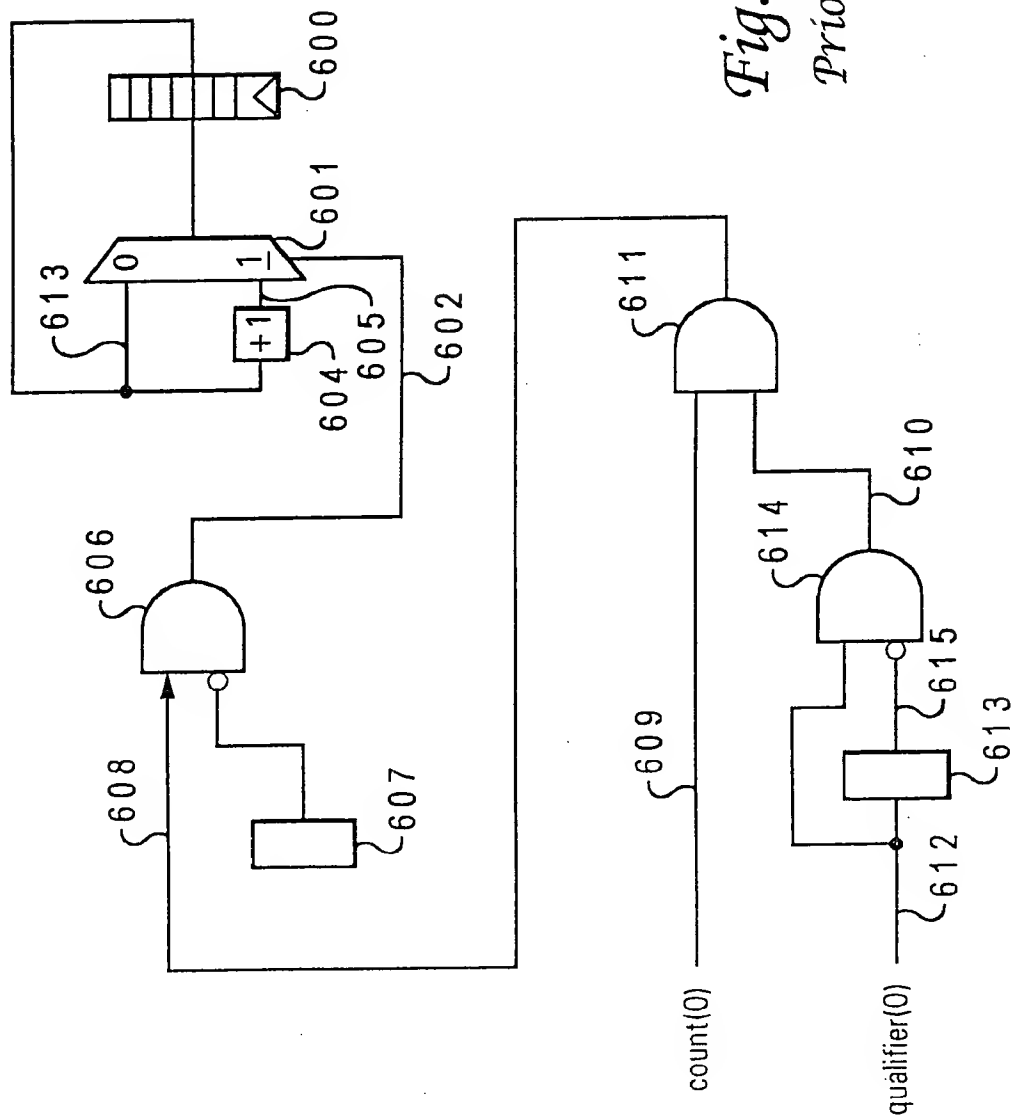


Fig. 6A
Prior Art

15/62

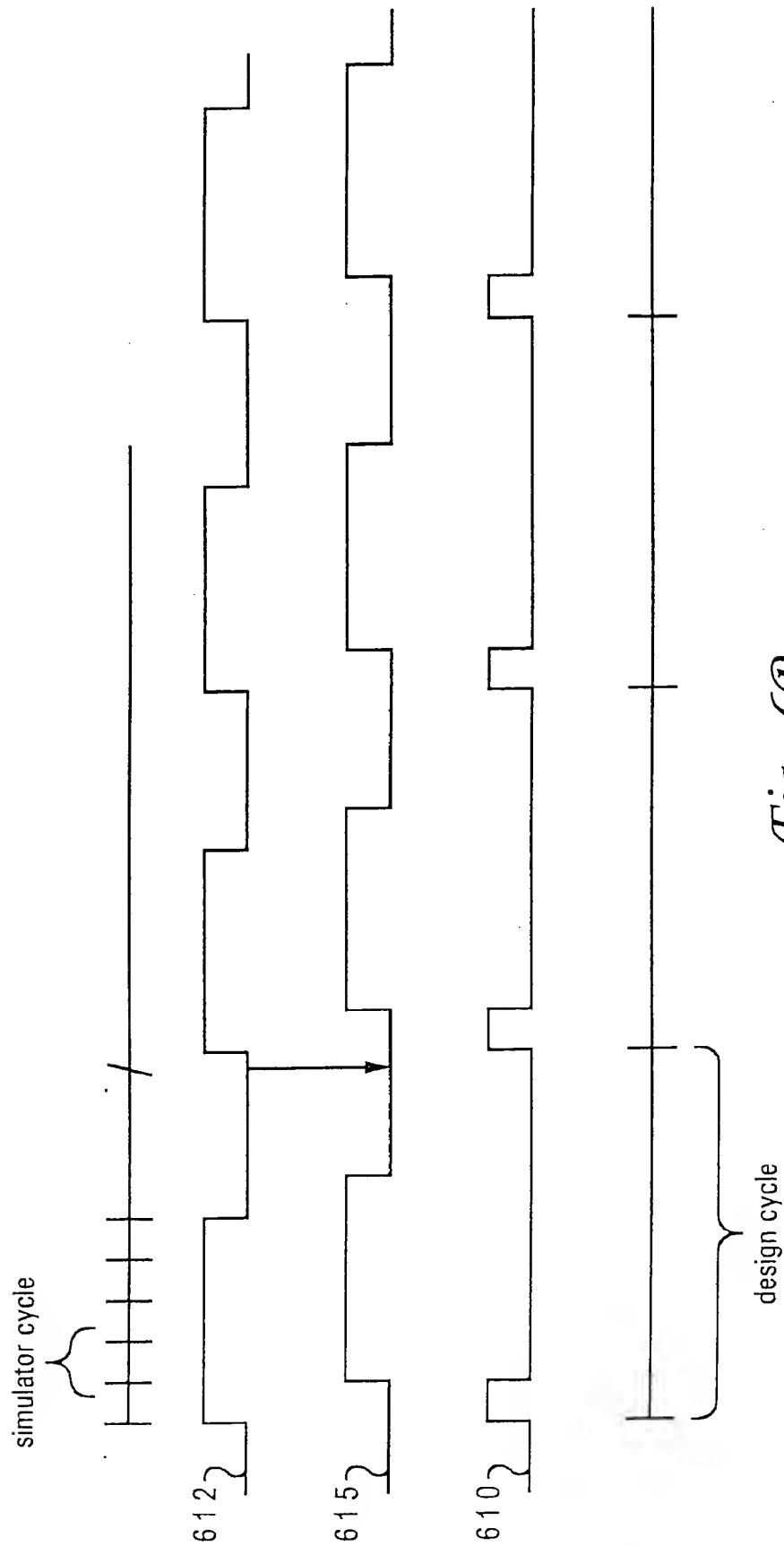


Fig. 6B
Prior Art

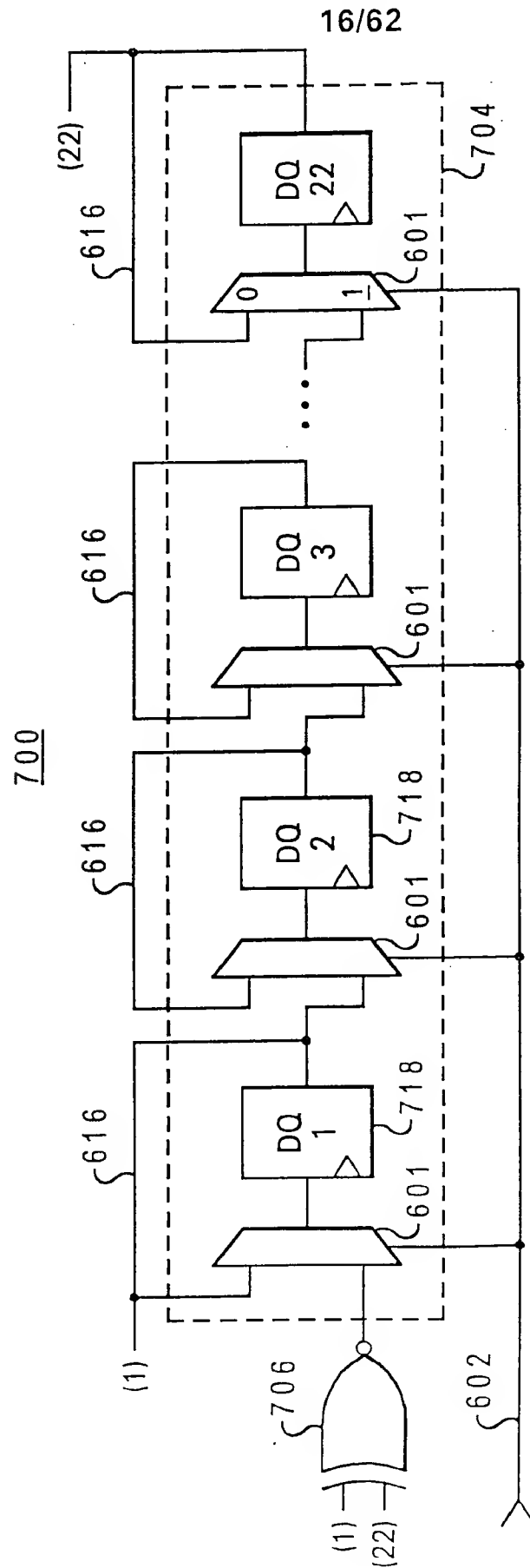


Fig. 7
Prior Art